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August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design ISLPED '99**

Publisher: ACM Press

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James Goodman, Anantha Chandrakasan, Abram P. Dancy

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3 Conserving network processor power consumption by exploiting traffic variability

Yan Luo, Jia Yu, Jun Yang, Laxmi N. Bhuyan

March 2007 **ACM Transactions on Architecture and Code Optimization (TACO)**, Volume 4 Issue 1

Publisher: ACM Press

Full text available: pdf(595.99 KB) Additional Information: full citation, abstract, references, index terms

Network processors (NPs) have emerged as successful platforms for providing both high performance and flexibility in building powerful routers. Typical NPs incorporate multiprocessing and multithreading to achieve maximum parallel processing capabilities. We observed that under low incoming traffic rates, processing elements (PEs) in an NP are idle for most of the time but still consume dynamic power. This paper develops a low-power technique to reduce the activities of PEs in accordance with ...

Keywords: Network processor, clock gating, low power, scheduling

4 Application specific processors: A low power architecture for embedded perception

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